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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,091	11/28/2001	Hayden Clavie Cranford JR.	RAL920010004US2 (IRA-10-5	2524

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,091	CRANFORD ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the appeal brief filed on 31 May 2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 3, 4, 7, 8, 13, 14, 17, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3 and 13 recite the limitations of using registers. However, both the specification (See Page 5 Paragraph 2) and the drawings (See Figure 2 Number 28) disclose using latches. It is unclear if the Applicant intends for registers and latches to be interpreted as functionally equivalent devices. For the purpose of evaluating prior art, the Examiner will assume that registers and latches perform an equivalent function.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1, 5, 6, 9, 10, 11, 15, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent number 5,115,450 to Arcuri ("Arcuri") and US Patent Number 5,943,378 to Keba et al. ("Keba").

7. In reference to Claim 1, Arcuri teaches a method of transferring stored digital parallel data of multiple bits of data stored in a first data register (See Figure 4 Number 54) from a transmitter (See Figure 3 Number 20) to a receiver (See Figure 3 Number 21) over a hard wired conductor (See Figure 3 Number 23) comprising the steps of: synchronously converting said stored digital data to a serial analog data signal in said transmitter (See Figure 4 Number 57); transmitting said serial signal asynchronously over said hard wired conductor to said receiver (See Column 3 Lines 48-52); and restoring said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter (See Figure 5 Number 83). Arcuri does not teach detecting both edges of the data in said asynchronous serial signal for conversion to parallel data bits and using a phase rotator to convert said asynchronous signal to said synchronous digital parallel data in conjunction with said edge detection. Arcuri teaches an analog to digital converter (See Figure 5 Number 83), but is silent as to the construction of it. Keba teaches a system that performs serial analog to parallel digital conversion (See Column 2 Lines 57-62) on a received signal using a symbol recovery unit (See Figures 1 and 3 Number 112) which comprises and edge detection unit for detecting both edges of the data (See Figure 3 Number 220, Column 4 Lines 55-56, and Column 5 Lines 2-5) and a

phase rotator working in conjunction with the edge detector for converting the asynchronous signal to a synchronous signal (See Figure 3 Number 225,Column 3 Lines 51-65, and Column 5 Lines 8-12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Arcuri using the symbol recovery unit of Keba to perform analog to digital conversion, resulting in the invention of Claim 1, because it is a conventional manner for optimizing the clock to have its positive edges near the center of each symbol period (See Column 3 Lines 53-57 and Column 5 Lines 10-12 of Keba), because it synchronizes the clock with less jitter than other symbol recovery techniques (See Column5 Lines 12-15 of Keba), and because it can be used as an alternative to an analog to digital converter (See Column11 Lines 4-7 of Keba).

8. Claim 11 recites limitations which are substantially equivalent to those of Claim 1, and thus is rejected under similar reasoning as applied to Claim 1 above.

9. In reference to Claim 5, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri further teaches that the data in the first register is comprised of eight bits (See Figure 8 Number 200).

10. Claim 15 recites limitations which are substantially equivalent to those of Claim 5, and thus is rejected under similar reasoning as applied to Claim 15 above.

11. In reference to Claim 6, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri further teaches that a clocking signal is used to convert the analog serial signal to a digital signal (See Figure 5 Number 80).

12. Claim 16 recites limitations which are substantially equivalent to those of Claim 6, and thus is rejected under similar reasoning as applied to Claim 16 above.

13. In reference to Claim 9, Arcuri and Keba teach the limitations as applied to Claim 1 above. Keba further teaches that edges are derived from multiple samples (See Column 4 Lines 4-13).

14. Claim 19 recites limitations which are substantially equivalent to those of Claim 9, and thus is rejected under similar reasoning as applied to Claim 9 above.

15. In reference to Claim 10, Arcuri and Keba teach the limitations as applied to Claim 9 above. Keba further teaches that the multiple samples are used to determine the approximate center of the resulting data bit (See Column 5 Lines 8-12).

16. Claim 20 recites limitations which are substantially equivalent to those of Claim 10, and thus is rejected under similar reasoning as applied to Claim 10 above.

17. Claims 2, 3, 4, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcuri and Keba as applied to Claim 1 above, and further in view of US Patent Number 6,222,380 to Gerowitz et al. ("Gerowitz").

18. In reference to Claim 2, Arcuri and Keba teach the limitations as applied to Claim 1 above. Arcuri and Keba do not teach that the digital parallel data is read out of the first data register into at least one single bit latch. Arcuri teaches parallel to serial conversion but is silent as to how it is performed. Gerowitz teaches a parallel to serial converter that reads data into at least one single bit latch (See Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Arcuri and Keba using the parallel to serial conversion device of Gerowitz, resulting in the invention of Claim 2, in order to allow the data to be transmitted over a high-speed, high-volume data path that uses fewer pins and transfers data at a faster rate than a traditional bus structure (See Column 2 Lines 16-20 of Gerowitz).

19. Claim 12 recites limitations which are substantially equivalent to those of Claim 2, and thus is rejected under similar reasoning as applied to Claim 2 above.

20. In reference to Claim 3, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 2 above. Gerowitz further teaches that the data is read N bits at a time (See Figure 2 D0-D3), each data bit to a different one of the N registers (See Figure 2

LATCH L1 – LATCH L4), and from each register to another register (See Figure 2 LATCH L5), and clocking an additional N bits of data to be subsequently written to said N registers and to said another register until all bits of data have been read (See Column 4 Line 64 – Column 5 Line 4). Arcuri, Keba, and Gerowitz do not expressly teach that the data is read out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit registers, and from each first and second single bit data register to a third single bit data register, clocking additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register. Gerowitz shows an exemplary embodiment where N is equal to 4; however, N can represent any integer, including 2. The portion of the specification describing the use of two single bit registers states that "It is to be understood that other than two bits at a time can be read from the register 24. However this number must be a number that is evenly divisible into the number of bits in the register 24."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to read the data out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit registers, and from each first and second single bit data register to a third single bit data register, clock an additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register, resulting in the invention of Claim 3, because Applicant has not disclosed that the use of two registers provides an advantage, is used for a particular

purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the four registers in the exemplary embodiment taught by Gerowitz or the two registers taught by Applicant because both perform the same function of converting a parallel data signal to a serial data signal, and because the N registers taught by Gerowitz can represent any integer number of registers. Therefore, it would have been obvious to one of ordinary skill in the art to modify Arcuri, Keba, and Gerowitz to obtain the invention as specified in Claim 3.

21. Claim 13 recites limitations which are substantially equivalent to those of Claim 3, and thus is rejected under similar reasoning as applied to Claim 3 above.

22. In reference to Claim 4, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 3 above. Gerowitz further teaches that the bits from the third single bit register are converted to a single serial analog signal of the data (See Figure 2 Signal Q and Column 5 Lines 5-15).

23. Claim 14 recites limitations which are substantially equivalent to those of Claim 4, and thus is rejected under similar reasoning as applied to Claim 14 above.

24. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcuri, Keba, and Gerowitz as applied to Claim 3 above, and further in view of US Patent Number 5,202,979 to Hillis et al. ("Hillis").

25. In reference to Claim 7, Arcuri, Keba, and Gerowitz teach the limitations as applied to Claim 3 above. Arcuri, Keba, and Gerowitz do not teach said analog signal is converted in said receiver to two one-bit signals and delivered to a shift register and then stored in a second data register. Arcuri further teaches storing the converted bits in said second data register (See Figure 5 Number 85). Arcuri teaches serial to parallel conversion (See Figure 5) but is silent as to how it is accomplished. Hillis teaches a shift register that takes two bits from a serial input signal and shifts them two bits at every clock pulse before shifting the accumulated bits out in parallel (See Figure 3 Number 34 and Column 3 Line 49 – Column 4 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Arcuri, Keba, and Gerowitz with the 2 bit shift register of Hillis, resulting in the invention of Claim 7, in order to speed up data transfer by only needing half as many clock pulses to accumulate the data from the input line (See Column 4 Lines 8-10 of Hillis), as well as to reduce power consumption since fewer clock transitions are required.

26. Claim 17 recites limitations which are substantially equivalent to those of Claim 7, and thus is rejected under similar reasoning as applied to Claim 7 above.

27. In reference to Claim 8, Arcuri, Keba, Gerowitz, and Hillis teach the limitations as applied to Claim 7 above. Arcuri further teaches that data bits are delivered synchronously to the second data register (See Figure 5 Numbers 77, 79, 80, and 81).

28. Claim 18 recites limitations which are substantially equivalent to those of Claim 8, and thus is rejected under similar reasoning as applied to Claim 8 above.

Conclusion

29. The following art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 5,131,013 to Choi; US Patent Number 5,757,862 to Ishizu; US Patent Number 5,936,678 to Hirashima; US Patent Number 6,731,697 to Boccuzzi et al.; US Patent Application Publication Number 2005/0111536 to Cranford et al.; US Patent Application Publication Number 2004/0066871 to Cranford et al.; US Patent Application Publication Number 2002/0146084 to Cranford et al.; US Patent Application Publication Number 2002/0136343 to Cranford et al.; and US Patent Application Publication Number 2002/0094055 to Cranford et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-

3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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